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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 07/14/2004

29

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/120,126	BAYS ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *February 23, 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 12-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 12-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The enclosed detailed action is in response to the Amendment submitted on February 23, 2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 17-19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Persaud (GBPN: 2074762) in view of Luan (USPN: 5,911,149).

Regarding claims 1-5, Persaud discloses an external (with respect to the agents) non-dedicated memory (*comprised of the master and slave memory portions collectively*) including a plurality of memory banks (*all of the memory chips for the master and slave memory portions; Page 8, Lines 57-58, wherein each memory chip is a memory bank*);

a first agent (*master processor/clock generator; Figure 4, Reference (s) 76, 78,126*) providing a first agent clock signal (*Figure 1; Reference 46 - master Continuous 02; Page 5, Lines 2-4*) adapted to control access to a first portion of the non-dedicated memory (*memory located on the master card; Page 1, Lines 44-45*) including a first number of the plurality of memory banks (*the memory chips on the master card, Page 8, Lines 57-58*); and

agent clock signal from the first agent (*Page 3, Lines 15-17, Page 5, Lines 2-4*), and providing a second agent clock signal which is synchronized to and in phase with the first agent clock signal (*the clock generator on the card with the slave processor receives the Bus Continuous 02 signal from the master and generates a local Continuous 02 signal having a representation of the bus continuous 02 signal, refer to Figure 9A - (3) and (8); Page 5, Line 2, Lines 26-33; Figure 1 shows the Continuous 02 signal output on line 46 from Reference 78*) to access a second portion of the non-dedicated memory (*the slave processor's corresponding memory portion; Page 1, Line 44*) including a second number of the plurality of memory banks (*the memory located on the slave card, comprised of eight chips; Page 8, Lines 57-58*). *Additionally, the external memory is not used as a dedicated memory. It is used as a common memory, wherein each slave processor has access to a portion of the memory and the master processor has access to the all of the memory. The Continuous 02 signals are used to generate the CAS and RAS signals (refer to Figures 1 and 2) which are used to access the memory (Figure 5, Reference 190), therefore the Continuous 02 signals are used to access the memory.* Persaud does not explicitly disclose the first and second number of the plurality of memory banks being variable nor does Persaud disclose a register to set at least one of the first and second number with a value set to correspond to a first number of the plurality of memory banks and a second number which is a remainder of the plurality of memory banks after the first number of the plurality of memory banks, which is adapted to be set by either one of the agents. However, Luan teaches the concept of a first and second memory portion comprising a first and second number of memory banks wherein the first and second number of memory banks are variable (*C 4, L 18-28; since the memory banks are dynamically allocated to the first and second portion, it is clear that the number of banks in the*

first and second memory portions are variable), and a register to set at least one of the first and second number of memory banks (***claim 2*** *- Figure 5, Reference 501*) with a value set to correspond to a first number of the plurality of memory banks (***claim 4*** *- value comprised of all the bits (bits 5:0) which are set [1]; Table 3; C 6, L 56-59; C 7, L 15-25*) and a second number which is a remainder of the plurality of memory banks after the first number of the plurality of memory banks (***claim 5***- *value comprised of all the bits which are not set [0]; Table 3; C 6, L 56-59; C 7, L 15-25*), which is adapted to be set by either one of the agents (***claim 3*** *- C 4, L 29-31, L 38-48; agents Figure 2, References 101 & 106*). In Persaud's system the number of banks in the first and second memory portions are fixed. Luan teaches that the use of a fixed memory architecture degrades the memory system capability and increases the overall memory cost in a computer system when the fixed portions of memory are under-utilized (C 1, L 13-43). Luan teaches that variable number of memory banks and the features cited above used to implement the variable memory banks (dynamic memory allocation) provide flexibility in the memory system configuration which allows the selecting of a size of the memory space to improve memory utilization given the current system configuration and the type of tasks to be performed (C 4, L 18-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings of Luan in the system taught by Persaud for the desirable purpose of flexibility and for improving the memory system capability and utilization. Additionally, Persaud does not explicitly disclose a synchronous memory. Persaud discloses a DRAM (*Figure 5, Reference 190*). Synchronous memories are well known in the art for operating at high speeds thus decreasing the bottleneck in computing systems associated with slow memory devices. Therefore it would have been obvious to one of ordinary skill in the art to

use a synchronous memory such as a SDRAM in Persaud's system for increased speed and improved performance.

Regarding claim 6, Persaud discloses the limitations cited above in claim 1, however, Persaud does not disclose the first and second agents as digital signal processors. Persaud discloses the first and second agents as microprocessors, such as the Motorola 6800 (*Figure 4, Reference 126*). Official notice is taken that digital signal processors are well known in the art for processing real world signals (represented by a sequence of numbers) using mathematical techniques to perform transformations or extract information, which provides advanced mathematical processing than a general microprocessor. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use digital signal processors in the system taught by Persaud for the desirable purpose of providing advanced mathematical processing for applications requiring extensive mathematical processing.

Regarding claims 17-19 and 22, Persaud discloses providing a memory access clock signal (*bus/master continuous 02 signal*) from a first agent (***claim 19***; *Page 3, Lines 15-17, Page 5, Lines 2-4; first agent is comprised of master processor/clock generator; Figure 4, Reference (s) 76, 78,126*);
providing a presentation of the memory access clock signal (*slave continuous 02 signal*) in synchronism and in phase with the memory access clock (*Page 2, Lines 45-47, Lines 52-55; Page 5, Line 2, Lines 26-33; Figure 1 shows the Continuous 02 signal output on line 46 from Reference 78; Page 5, Line 2, Lines 16-33; Page 6, Line 6-51; Figures 9A-9D and 10; Page 6, Lines 46-65; Page 7, entirety; Page 8, Lines 1-22, Lines 34-46 - Persaud teaches that all of the mpu 02 signals are synchronized to each other. The Bus Continuous 02 signal and the slave*

continuous 02 are the same signals as the master mpu 02 signal and the slave mpu 02 signal respectively. The master mpu 02 signal and the slave mpu 02 signals are synchronized to each other and thus so is the slave continuous 02 signal and the bus/master continuous 02 signal);
regenerating in a second agent (*one of the slave processors/clock generator; Figure 4, Reference(s) 76, 78, 126 located in Reference 14 in Figure 3; Page 4, Lines 5-10; Page 1, Line 42*) the memory access clock signal (***claim 18** - Page 5, L 2, L 16-33; Page 6, L 6-51; Figures 9A-9D and 10; Page 6, L 46-65; Page 7, entire; Page 8, L 1-22, L 34-46*);
firstly accessing a portion (*part of the shared memory corresponding to an address of a memory request by the master processor*) of the external non-dedicated shared memory (*comprised of one of the slave memories; Page 1, Lines 44-45*) from the first agent based on the memory access clock signal (*Page 1, L 44-45; Page 2, Lines 1-7; Pages 9-10 with respect to Figure 11; Page 11, 49-58; Page 12, Lines 1-19*);
secondly accessing a portion (*part of the shared memory corresponding to an address of a memory request by the slave processor*) of the external non-dedicated shared memory from a second agent based on the representation (regenerated) of the memory access clock signal (*Page 1, L 44-45; Pages 9-10 with respect to Figure 11- The slave Continuous 02 signal is used to generate the CAS and RAS signals (refer to Figures 1 and 2) which are used to access the shared memory (Figure 5, Reference 190 located on one of the slave cards), therefore the Continuous 02 signal is used to access the memory. The continuous 02 signal is generated based on the bus continuous 02 and therefore, the first agent memory access is based on the memory access clock);*
wherein the secondly accessing follows said firstly accessing without a wait state there between (*Page 1, Lines 46-49; Page 3, Lines 47-61; Persaud teaches that the slave processor is inhibited from accessing the shared memory only during the clock cycle(s) in which time the master is*

accessing the shared memory, which means that the slave accesses the shared memory immediately after the master. Hence no wait states are used or required).
The shared memory is located externally to the agent and it is not used as a dedicated (unshared, private) memory because it is shared between the two agents. Persaud does not explicitly disclose a synchronous memory. Persaud discloses a DRAM (*Figure 5, Reference 190*). Synchronous memories are well known in the art for operating at high speeds thus decreasing the bottleneck in computing systems associated with slow memory devices. Therefore it would have been obvious to one of ordinary skill in the art to use a synchronous memory such as a SDRAM in Persaud's system for increased speed and improved performance.

4. Claims 7-8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (USPN: 5,659,715) in view of Persaud (GBPN: 2074762).

Regarding claims 7-8, Wu discloses a plurality of agents (system controller and graphics controller)(C 4, L 58-65); an external non-dedicated shared asynchronous memory block accessible by each of the plurality of agents (C 7, L 1-65); a register adapted to partition the external non-dedicated shared memory block into a plurality of partitions, each plurality of partitions being accessible by a unique group of the plurality of agents (C 9, L 23-52). Wu does not explicitly disclose the shared memory block comprising a plurality of memory banks. However, it is common knowledge in the art for memory to comprise a plurality of banks or blocks. Such as system memory (DRAM, SDRAM etc.) in a computing system. Wu teaches the concept of dynamically allocating portions of memory to a first and second agent such that the performance of the memory is improved. One of ordinary skill in the art would have recognized the benefits of Wu's teachings and would have been motivated to use the teachings of Wu in a

memory comprising a plurality of banks for the desirable purpose of flexibility and improved performance. Additionally, Wu does not disclose a plurality of agents each receiving a common base clock signal from another agent and accessing the external non-dedicated shared memory with a memory access signal synchronized and in phase with the common base clock signal. However, Persaud teaches the concept of providing a master clock (base clock) from a master processor (first agent) to slave processors (plurality of agents) to synchronize the slaves' circuitry to the master clock to provide reliable and accurate data transfers between the master processor and the slave processor (s) by accessing the external non-dedicated shared memory with a memory access signal synchronized and in phase with the common base clock signal (Page 1, Lines 39-65, Page 3, L 1-22). One of ordinary skill in the art would have recognized the efficient use of memory provided by Wu's teachings and would have been motivated to use such teachings in a synchronous system using the features taught by Persaud for the desirable purpose of efficiency and improved performance.

Regarding claim 12, neither Wu nor Persaud disclose a SDRAM. However, synchronous memories are well known in the art for operating at high speeds thus decreasing the bottleneck in computing systems associated with slow memory devices. Therefore it would have been obvious to one of ordinary skill in the art to use a SDRAM in the system taught by Wu and Persaud for increased speed and improved performance.

5. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Persaud (GBPN: 2074762) in view of Muthal (USPN: 5,815,167).

Regarding claims 13 and 15, Persaud discloses a first agent (*master processor/clock generator; Figure 4, Reference (s) 76, 78,126*) to provide a first agent memory access clock signal (*Figure 1; Reference 46 - master Continuous 02; Page 5, Lines 2-4*) to allow the first agent to access the shared external non-dedicated memory (*comprised of one of the slave memories; Page 1, Lines 44-45; Page 2, Lines 1-7; the bus/master continuous 02 signal is used to synchronize the slave clock generator to the master clock generator so that the master may suspend the operations of the slave processor so that the master can access the shared memory (Page 2, Lines 52-55). Hence the bus/master continuous 02 signal allows the first agent to access the shared external non-dedicated memory);*

and a second agent (*one of the slave processors/clock generator; Figure 4, Reference(s) 76, 78, 126 located in Reference 14 in Figure 3; Page 4, Lines 5-10; Page 1, Line 42*), receiving the first agent memory access clock signal from the first agent (*Page 3, Lines 15-17, Page 5, Lines 2-4*), and providing a second agent memory access clock signal (*the clock generator on the card with the slave processor receives the Bus Continuous 02 signal from the master and generates a local Continuous 02 signal having a representation of the bus continuous 02 signal, refer to Figure 9A - (3) and (8); Page 5, Line 2, Lines 26-33; Figure 1 shows the Continuous 02 signal output on line 46 from Reference 78*) to access the shared external non-dedicated memory in synchronism with the access by the first agent to the shared external non-dedicated memory (*Page 1, Line 44; Page 2, Lines 45; Page 3, Lines 15-22*). *The shared memory is non-dedicated because it is accessible by both of the agents. Also, Persaud teaches that the slave processor operations [memory accesses, etc.] are synchronized to the operations of the master processor. The slave clock generator, which is synchronized to the master clock generator, generates a local*

Continuous 02 signal which is used to generate the RAS and CAS signals for accessing the memory, having the same clock cycle and phase as the master Continuous 02 signal. Hence the slave processor accesses the shared memory in synchronism with the master access to the shared memory. Persaud does not teach the first agent and the second agent accessing different portions of the shared external non-dedicated memory simultaneously. However, Muthal teaches the concept of simultaneous access to a shared memory by a plurality of agents, wherein the shared memory is partitioned such that a first agent accesses has access to a first partition (DRAM row 220.1) and a second agent has access to a second partition (DRAM row 220.2) (**claim 15**) (*Figure 2, C 5, L 35-67; C 6, L 17-24; Abstract*). Muthal teaches that this feature increases the effective memory bandwidth of a computer system (*C 8, L 20-30*). In Persaud's system either the master or the slave processor is accessing the memory at one time which may affect the throughput of the system (*Page 1, Lines 46-49; Page 2, Lines 22-29*). One of ordinary skill in the art at the time the invention was made would have recognized the shortcomings of Persaud's system and would have been motivated to use the teachings of Muthal with the Persaud's system for the desirable purpose of increasing the throughput and performance of the system. Additionally, Persaud does not explicitly disclose a synchronous memory. Persaud discloses a DRAM (*Figure 5, Reference 190*). Synchronous memories are well known in the art for operating at high speeds thus decreasing the bottleneck in computing systems associated with slow memory devices. Therefore it would have been obvious to one of ordinary skill in the art to use a synchronous memory such as a SDRAM in Persaud's system for increased speed and improved performance.

Regarding claim 14, Persaud discloses the shared memory servicing in turn the first agent and the second agent without a wait state there between (*Page 1, Lines 46-49; Persaud teaches that the slave processor is inhibited from accessing the shared memory for one clock cycle during which time the master is accessing the shared memory, which means that the slave continues to access the shared memory after the one clock cycle which does not include any wait states*).

Regarding claim 16, Persaud discloses the limitations cited above in claim 13, however, Persaud does not disclose the first and second agents as digital signal processors. Persaud discloses the first and second agents as microprocessors, such as the Motorola 6800 (*Figure 4, Reference 126*). Official notice is taken that digital signal processors are well known in the art for processing real world signals (represented by a sequence of numbers) using mathematical techniques to perform transformations or extract information, which provides advanced mathematical processing than a general microprocessor. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use digital signal processors in the system taught by Persaud for the desirable purpose of providing advanced mathematical processing for applications requiring extensive mathematical processing.

6. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (USPN: 5,659,715) in view of Persaud (GBPN: 2074762).

Regarding claim 20, Wu discloses setting a configuration register to partition the external non-dedicated shared memory into a first partition and a second partition (*C 9, L 23-59; C 10, L 1-30;*

partitions- address ranges allocated to the graphics and system controllers; register - storage which stores the address ranges assigned to the system controller and the graphics controller); accessing a first portion of memory from a first agent (*graphics controller - C 4, L 58-65*); accessing a second portion of memory from a second agent (*system controller - C 4, L 58-65*); and repartitioning the shared memory on the fly (*C 7, L 11-23*). Wu does not disclose the external shared memory partitions comprising a plurality of memory banks. However, official notice is taken that memory comprising a plurality of banks (modules) is well known in the art, particular for providing a large storage capacity. Wu teaches the concept of dynamically allocating portions of a memory bank to a first and second agent such that the performance of the memory is improved. Thus, it would have been obvious to one of ordinary skill in the art to add a plurality of banks to the system taught by Wu for the desirable purpose of increasing the storage space to provide the storage capacity required for a system's design requirements. Additionally, Wu does not disclose a second agent receiving a clock representation from the first agent and generating a second agent clock signal for said second agent's access to the non-dedicated shared memory. However, Persaud teaches the concept of providing a clock representation of a master clock (bus continuous 02) to a second agent to synchronize the slaves' circuitry (second agent) to the master's circuitry (first agent) to provide reliable and accurate data transfers between the master processor and the slave processor (s) by generating a second clock agent signal for said second agent's access to the non-dedicated memory (slave continuous 02 signal) (*Page 1, Lines 39-65, Page 3, L 1-22; Page 5, Lines 2-4*). Therefore, it would have been obvious to one of ordinary skill in the art to use the teachings of Persaud with the teachings of Wu for the desirable purpose of ensuring reliable and accurate data transfers. Persaud does not

explicitly disclose a synchronous memory [synchronous memory banks]. Persaud discloses a DRAM (*Figure 5, Reference 190*). Synchronous memories are well known in the art for operating at high speeds thus decreasing the bottleneck in computing systems associated with slow memory devices. Therefore it would have been obvious to one of ordinary skill in the art to use a synchronous memory such as a SDRAM in Persaud's system for increased speed and improved performance.

Regarding claim 21, Wu discloses the first agent (graphics controller) performing the repartitioning (reallocation) (*C 6, L 66-67; C 7, L 1-10*).

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (USPN: 5,659,715).

Regarding claim 23, Wu discloses setting a configuration register to partition the external non-dedicated shared memory into a first partition and a second partition (*C 9, L 23-59; C 10, L 1-30; partitions- address ranges allocated to the graphics and system controllers; register - storage which stores the address ranges assigned to the system controller and the graphics controller*); accessing a first portion of memory from a first agent (*graphics controller - C 4, L 58-65*); accessing a second portion of memory from a second agent (*system controller - C 4, L 58-65*); and repartitioning the shared memory on the fly (*C 7, L 11-23*). Wu does not disclose means for accessing the second partition from a second agent that receives a clock signal from the first agent and generates a second agent clock signal in synchronism and in phase with the received clock signal, for the second agent's access to the shared memory. However, Persaud teaches the

concept of providing a first clock (base clock) from a master processor (first agent) to slave processors (plurality of agents) to synchronize the slaves' circuitry to the master clock to provide reliable and accurate data transfers between the master processor and the slave processor (s) by generating clock signals in synchronism and in phase the first clock signal for accessing the shared memory (Page 1, Lines 39-65, Page 3, L 1-22). One of ordinary skill in the art would have recognized the efficient use of memory provided by Wu's teachings and would have been motivated to use such teachings in a synchronous system using the features taught by Persaud for the desirable purpose of efficiency and improved performance.

Additionally, Wu does not disclose the external shared memory partitions comprising a plurality of memory banks. However, official notice is taken that memory comprising a plurality of banks (modules) is well known in the art, particular for providing a large storage capacity. Wu teaches the concept of dynamically allocating portions of a memory bank to a first and second agent such that the performance of the memory is improved. Thus, it would have been obvious to one of ordinary skill in the art to add a plurality of banks to the system taught by Wu for the desirable purpose of increasing the storage space to provide the storage capacity required for a system's design requirements.

Response to Arguments

8. Applicant's arguments filed have been fully considered but they are not persuasive.

Regarding Applicant's argument that Persaud fails to teach synchronous memory and the use of synchronized clock signals accessing the same memory, the Examiner disagrees. The above rejection is a 35 U.S.C. 103 (a) rejection which indicates that all the features are not present in the primary rejection. The feature of a synchronous memory has been covered in the above 103 rejection and thus Applicant's argument that Persaud fails to teach a synchronous memory is not warranted. Additionally, the clock signals are synchronized via the use of the individual clock generator and the memory is accessed via such signals. Hence, Persaud does teach using synchronized clock signals to access a memory and the 103 rejection above discloses the use of synchronous memories.

The Applicant has made the assertion that synchronization signals applied over a backplane are not clock signals. There is no evidence provided to support such an assertion. A clock signal is a clock signal irregardless to whether it is applied over a backplane or not. The way a signal is routed does not prevent it from being a clock signal.

The fact that Persaud's design is old does not prevent such design from disclosing the claimed invention, in fact it goes to establish that Applicant's claimed features were known for a long time.

Regarding Applicant's arguments with respect to the teachings of Luan, Luan is relied upon for teaching variably sized memory banks and it is not relied upon for teaching routing clock signals. Hence, Applicant's arguments are incommensurate with the above rejection.

Regarding Applicant's arguments with respect to the teachings of Wu, Wu is not relied upon for teaching receiving a clock signal from another agent and accessing a synchronous memory with such and thus Applicant's arguments are incommensurate with the above rejection.

Applicant's arguments with respect to the teachings of Muthal are incommensurate with the above rejection.

The arguments presented by the Applicant appear to argue the rejection in a manner inconsistent with the type of rejection made. The references relied upon other than Persaud are not relied upon for teaching receiving or generating a signal synchronized to the received signal for accessing a memory. This feature is taught by Persaud as stated above.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

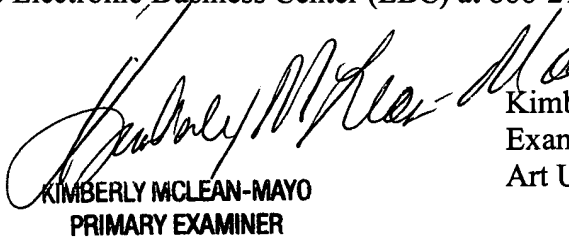
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M (10:00 - 6:30); Tues, Thr (10:00 - 4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

July 10, 2004